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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/691,033	10/19/2000	Atsushi Kunimatsu	198765US2	5152

22850 7590 03/24/2005

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EXAMINER	
BULLOCK JR, LEWIS ALEXANDER	
ART UNIT	**PAPER NUMBER**
2195	4

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/691,033	KUNIMATSU ET AL.	
	Examiner	Art Unit	
	Lewis A. Bullock, Jr.	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-27 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-27 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 1/19/01.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over REEVE (U.S. Patent 5,535,393) in view of ROSTOKER (U.S. Patent 5,761,516).

As to claim 1, REEVE teaches a parallel computer (parallel processing apparatus) having a hierarchy structure comprising: an upper processing unit (level 2 segment / level 1 segment) for executing a parallel processing task in parallel; and a plurality of lower processing units (level 0 segments) connected to the upper processing unit through a connection line (bus element), wherein the upper processing unit divides the parallel processing task (sequence) to a plurality of subtasks (subtasks), and assigns the plurality of subtasks (subtasks) to the corresponding lower processing units and transfers data to be required for executing the plurality of subtasks to the lower processing units (via division and allocation of instructions and data), and the lower processing units execute the corresponding subtasks from the upper processing unit (see fig. 1; col. 5, lines 22-42; col. 2, lines 1-17; col. 44, lines 1-27; col. 44, line 57-61). However, REEVE does not mention that the processor informs upon the completion of the task.

ROSTOKER teaches a multiprocessor system in any type of architecture (col. 3, lines 9-16, lines 32-42) wherein a parent processor distributes a subtask of an overall task to another processor for execution wherein the results are returned to the parent processor (via a callback) (col. 5, line 40 – col. 6, line 38; col. 4, lines 46-55). Therefore, it would be obvious to one skilled in the art at the time of the invention to combine the teaching of REEVE with the teachings of ROSTOKER in order to facilitate improved price performance than conventional multi-chip designs (col. 2, lines 5-9).

As to claim 2, REEVE teaches a parallel computer (parallel processing apparatus) having a hierarchy structure comprising: an upper processing unit (level 2 segment) for executing a parallel processing task in parallel; a plurality of intermediate processing units (level 1 segment) connection to the upper processing unit through a first connection line (bus segment); and a plurality of lower processing units (level 0 segments) connected to the intermediate processing units through a second connection line (bus segments), wherein the upper processing unit divides the parallel processing task (sequence) to a plurality of first subtasks (subtasks), and assigns the plurality of first subtasks to the corresponding intermediate processing units, and transfers data to be required for executing the plurality of first subtasks to the intermediate processing units (level 1 segments), and the intermediate processing units divide the first subtasks (tasks) to the plurality of second subtasks (subtasks), and assigns the plurality of second subtasks to the corresponding lower processing units, and transfers data (via division and allocation of instructions and data) to be required for executing the plurality

of second subtasks to the lower processing units, and the lower processing units execute the corresponding second subtasks (via processors executing the subtasks). (see fig. 1; col. 5, lines 22-42; col. 2, lines 1-17; col. 44, lines 1-27; col. 44, line 57-61). However, REEVE does not mention that the processor informs upon the completion of the task.

ROSTOKER teaches a multiprocessor system in any type of architecture having a plurality of processors (col. 3, lines 9-16, lines 32-42) wherein a parent processor distributes a subtask of an overall task to another processor for execution wherein the results are returned to the parent processor (via a callback) (col. 5, line 40 – col. 6, line 38; col. 4, lines 46-55). It would be obvious from the teachings of ROSTOKER that each processor distributes the subtask and is returned the results via a callback between the initial processor and subsequent processors in a system with more than two processors are implemented. Therefore, it would be obvious to one skilled in the art at the time of the invention to combine the teaching of REEVE with the teachings of ROSTOKER in order to facilitate improved price performance than conventional multi-chip designs (col. 2, lines 5-9).

As to claims 3-27, ROSTOKER teaches the processors are different types having memory, with/without a DMA controller, and mounted on a multi-chip module on a board or separate multi-chip modules of a board connected via a bus, cross-bus, or any other network connection (col. 3, lines 9-52). In addition, ROSTOKER teaches the system wherein a parent processor distributes a subtask of an overall task to another processor

for execution wherein the results are returned to the parent processor (via a callback) (col. 5, line 40 – col. 6, line 38; col. 4, lines 46-55). It would be obvious from the teachings of ROSTOKER that each processor distributes the subtask and is returned the results via a callback between the initial processor and subsequent processors in a system with more than two processors are implemented. Therefore, it would be obvious to one skilled in the art at the time of the invention to combine the teaching of REEVE with the teachings of ROSTOKER in order to facilitate improved price performance than conventional multi-chip designs (col. 2, lines 5-9).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lewis A. Bullock, Jr. whose telephone number is (571) 272-3759. The examiner can normally be reached on Monday-Friday, 8:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng An can be reached on (571) 272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

March 21, 2005

LEWIS A. BULLOCK, JR.
PRIMARY EXAMINER